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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,894	ROOHPARVAR, FRANKIE F.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This application is a Divisional of U.S. Application Serial No. 09/608,257; now U.S. patent 6,785,765. Claims 1-20 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sredanovic et al. (USPN: 6,084,803); hereinafter Sredanovic, in view of Nizar et al. (USPN: 6,378,056); hereinafter Nizar.

As per claim 1; Sredanovic discloses the invention as claimed including a method for operating a synchronous memory comprising performing an initialization operation on the

synchronous memory is equivalently taught as performing an initialization operation on the synchronous memory by the command decoder 350, particularly the latch 110 which is part of the synchronous graphic random access memory (SGRAM) 310 (e.g. see figure 3, column 3, lines 55 et seq.); Sredanovic further discloses the mode register 360 for storing initialization values provided on address pins of terminal 340 (e.g. see column 3, lines 49 et seq.). Sredanovic discloses the invention as claimed except for setting a content of a status register to a first state while initialization operation is being performed and to a second state when initialization being completed. Nizar, in his teaching of method and apparatus for configuring memory devices, discloses ***control status register*** (being equivalent to status register as claimed) having an initialization opcode (IOP) field for storing the initialization operation; an initiate initialization operation (IIO) field wherein the IIO field, when being set to a first state, causing the control circuit to execute the initialization operation and then clear the IIO field to a second state; an initialization complete (IC) field for indicating whether an initialization process has completed (e.g. see column 4, lines 1-35; column 24, lines 60-67; also TABLE 2, description for bit 23). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the teaching of Nizar with the

utilization of the status register (or mode register 360) having multiple programmable data fields/bits for indicating of (a) execution of the initialization operation, and (b) initialization completion status wherein a content of the status register is set to a first state while initialization operation is being performed and set to a second state when initialization being completed. In doing so, it would allow for quick reference of system data if initialization would have occurred; for example, important system data can be quickly/reliably retrieved or backed-up, therefore enhancing system reliability. It also provides the ease of capturing of system start-up information such as system faults, system configuration through the usage said control status register, therefore being advantageous.

As per claim 2, the further limitation of initialization operation is performed in response to an externally provided signal is equivalently taught as the initialization operation being performed when a signal S is received from one or more terminals (e.g. see column 2, lines 45 et seq.); also by an external initialization signal SET, see abstract;

As per claim 3, the further limitation of outputting the contents of the status register on an external connection in response to a status register read command is taught by the combination of Sredanovic and Nizar, since Nizar, starting on column 3, lines 43 et seq., clearly discloses *the content of*

control registers can be read (and outputting to external connection) and written via the serial interface circuit 140;

As per claim 4, noting that Sredanovic discloses synchronous memory 310 comprising the programmable latch 110 having non-volatile fuse F1 (e.g. see column 1, lines 23 et seq.) and a register, wherein Sredanovic clearly discloses the initialization operation comprises writing the register with a parameter defining operation which is known to be from data reading-off from the non-volatile fuse F1 (e.g. see column 7, lines 37-40);

As per claim 5, Nizar discloses the first state is a logical 1 and the second state is a logical 0 (e.g. see TABLE 2, first paragraph description portion for bit 23);

As per claim 6, see arguments with respect to claims 1 and 3; in addition, the Nizar further discloses providing a status register (control register 112) read command with an external memory controller (control circuit 120) (e.g. see column 3, lines 29-38);

As per claim 7, noting that Sredanovic discloses synchronous memory 310 comprising the programmable latch 110 having non-volatile fuse F1 (e.g. see column 1, lines 23 et seq.) and a register, wherein Sredanovic clearly discloses the initialization operation comprises writing the register with a parameter defining operation which is known to be from data reading-off from the non-volatile fuse F1 (e.g. see column 7, lines 37-40);

As per claim 8, Sredanovic discloses the initialization operation being performed when a signal S is received from one or more terminals (e.g. see column 2, lines 45 et seq.); also by an external initialization signal SET from the memory controller or (command decoder 350), see Sredanovic's abstract, fig. 3;

As per claim 9 and 10, Sredanovic discloses the latch of synchronous memory 310 is non-volatile elements or flash memory (EPROM, EEPROM, UPROM etc... (e.g. see column 7, line 10);

As per claim 11; Sredanovic discloses the invention as claimed including a method for operating a memory system comprising initiating and initialization operation on a memory device is equivalently taught as performing an initialization operation on the synchronous memory by the command decoder 350, particularly the latch 110 which is part of the synchronous graphic random access memory (SGRAM) 310 (e.g. see figure 3, column 3, lines 55 et seq.); Sredanovic further discloses the mode register 360 for storing initialization values provided on address pins of terminal 340 (e.g. see column 3, lines 49 et seq.). Sredanovic discloses the invention as claimed except for monitoring a memory status register to determine when the initialization operation is completed. Nizar, in his teaching of method and apparatus for configuring memory devices, discloses ***control status register 112*** (being equivalent to status register as claimed) having an initialization opcode (IOP) field for

storing the initialization operation; an initiate initialization operation (IIO) field wherein the IIO field (e.g. see column 3, lines 29 et seq.); Nizar further discloses monitoring the register to determine the completion of the initialization (e.g. see column 4, lines 29-35). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the teaching of Nizar for that of Sredanovic wherein completion of initialization operation is determined by monitoring the status register by polling the IIO bit in order to arrive at the Applicant's current invention. In doing so, it would enhance system reliability by halting other operations to allow for system initialization to occur prior to stale data being accessed, it further allow initialization operation to occur in sequence, therefore being advantageous.

As per claim 12, the memory controller is equivalently taught as control circuit 120 for controlling/monitoring the initialization operation (e.g. see Nizar's column 3, line 30 bridging column 4, line 35);

As per claim 13; Sredanovic discloses the invention as claimed except for performing a status read command on the status register, determining state of a first bit of the status register and if the first bit is in a predetermined state, indicating the end (completion) of the initialization operation. Nizar, in his teaching of method and apparatus for configuring memory devices,

discloses performing a status read command on the control register (being equivalent to status register as claimed) wherein the ***control status register*** having an initialization opcode (IOP) field for storing the initialization operation; an initiate initialization operation (IIO) field; determining state of a first bit of the status register and if the first bit is in a predetermined state, indicating the end (completion) of the initialization operation is equivalently taught as the IIO field having first and second states, and when being set to a second state (0) for indicating of the completion of the initialization process (e.g. see TABLE 2, description for bit 23; column 4, lines 1-35). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the teaching of Nizar with the utilization of the status register having multiple programmable data fields/bits for indicating of (a) execution of the initialization operation, and (b) initialization completion status wherein a content of the status register is set to a first state while initialization operation is being performed and set to a second state when initialization being completed. In doing so, it would allow for quick reference of system data if initialization would have occurred; for example, important system data can be quickly/reliably retrieved or backed-up, therefore enhancing system reliability. It also provides the ease of

capturing of system start-up information such as system faults, system configuration through the usage said control status register, therefore being advantageous.

As per claim 14, see argument with respect to claim 14, in addition, it should be noted that further limitation of determining a state of a plurality of bits of the status register is taught by Nizar as bit 23 and 20 are being determined for initialization process completion status (e.g. see TABLE 2);

As per claim 15, the further limitation of outputting the contents of memory status register to a data output connection is taught by the combination of Sredanovic and Nizar, since Nizar, starting on column 3, lines 43 et seq., clearly discloses *the content of control registers can be read (and outputting to external connection) and written via the serial interface circuit 140;*

As per claim 16, Sredanovic discloses memory device 310 is an integrated synchronous graphics random access memory (SGRAM) (e.g. see column 3, lines 16 et seq.; figure 3);

As per claim 17, the combination of Sredanovic and Nizar discloses the status read command and determines the state of the plurality of bits is performed by the control circuit 120 (memory controller as being claimed) (e.g. see column 3, lines 30 et seq.);

As per claim 18, the further limitation of monitoring the

memory status register is performed by a memory controller (control circuit 120) over a bidirectional data [180] bus is taught by Nizar to the extent that it is being claimed (e.g. see figures 1 and 2; column 3, lines 7 et seq.);

As per claim 19; first of all, it's known in the data processing art that any control circuit can be implemented by digital logic design utilizing multiple states known as state machine, the combination of Sredanovic and Nizar disclose the initialization operation on the memory device is performed by control circuit 120 (e.g. see Nizar's column 3, lines 31 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the control circuit 120 as an internal state machine as being claimed, by using internal state machine as opposed to conventional analog implementation, it allow for quick and simplification in system control design and implementation; in addition, it would further allow the combined system of Sredanovic and Nizar to server broader range of application, therefore being advantageous;

As per claim 20, Nizar discloses the data register 114 stores updated status data relating to any particular initialization operation including the completion of the initialization operation (e.g. see column 4, lines 1 et seq.); in addition, the further limitation of synchronous with a clock

signal coupled to the memory device is taught by Nizar as clock generator 580 is utilized in initialization sequence to provide clock signals over signal line 582 (e.g. see figure 5, column 13, lines 20-51).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (703) 305-3842. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/October 10, 2004

Tuan V. Thai
PRIMARY EXAMINER
Group 2100